Abstract of the Disclosure:

A digitally controlled circuit for reducing the phase modulation of a signal. The circuit has a multiphase clock generator that produces n phases of a clock that is m-times the signal. The circuit further has a multiplexer with n inputs for the n phases of the clock and with one output which supplies the output signal. The output signal and the signal are connected to the inputs of a phase comparator. The output signal of the comparator is supplied to a sigma-delta modulator whose output signals are used for controlling the multiplexer. A jittered input signal is compared in the phase comparator with a master clock. The determined phase difference is integrated in a sigma-delta modulator. The aim of the circuit is to generate a clock without jitter, digitally and without using external components. This circuit provides 20 dB/decade attenuation of the jitter received in the SYNC signal, based on the P-regulator characteristic.

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